THE UNIVERSITY OF NEW MEXICO
Department of Physics and Astronomy

Progress Report

May 1, 1965 - October 31, 1965

NASA Grant NsG-332

[redacted]

"Measurement of High Energy Neutron Flux in Space"

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Summary of Progress

May 1, 1965 - Oct. 31, 1965

I. Scintillation Recoil Detector

The new detector arrangement described in the previous report was operated at Albuquerque and at mountain altitudes with the result that the expected improved performance was confirmed experimentally. A slightly revised design has been started which will conform to the space limitations of the OSO-G spacecraft. In addition, solid light pipes for the two convertor counters have been designed and are being tested. These are required for the satellite version to enable the phototubes to be fitted into the available space.

II. Circuitry

A. Pulse Height Digitizer. Design of a pulse height digitizer employing operational amplifiers has been completed. The method employed is efficient in its use of time and power, is inherently stable and simple. Since no height-to-time conversion is involved, a five-microsecond conversion time for full scale (eight bits) is readily attained. The circuit design outlined in Figure 1 has been analyzed by computor and is now being built for testing.

B. Preliminary OSO-G Circuit Design.

The design concepts required to adapt the experiment to the OSO-G spacecraft have been completed on a tentative basis and are shown in block form in Figure 2. All events are accepted for readout whether or not they are accompanied by a pulse in the anticoincidence counter. Neutron events (no anticoinc. pulse) are identified as such by a separate indicator bit. In order to prevent the comparatively high

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charged-particle rate from resulting in a large dead time for neutron events, priority is given to the neutron events. For example, if a proton event is digitized and stored in the shift registers awaiting readout when a neutron event occurs, the proton event is cleared out and the neutron event entered in.

Wheel azimuth pointing direction is indicated by the spacecraft sun pulse in conjunction with a timer. Each event is accompanied by an azimuth indication.

C. In-flight Calibration.

It has been decided to include a calibrate mode, initiated by command, in which a pulse height spectrum is obtained for each counter separately, with weak alpha sources being present as energy scale indicators.

III. Multiple Plate Ion Chamber

A. Chamber.

A single section of the multiple plate chamber has been built and tested. Pulse height spectra from alpha-particle sources were obtained which revealed unacceptably poor resolution. A new chamber with modified geometry is now under construction. The chamber with input circuit is shown in Figure 3.

B. Circuitry.

In order to operate an ion chamber under satellite conditions a high-gain, low-noise amplifier employing solid-state components and consuming minimum power must be used. Such a circuit was designed and constructed during this period. It employs field effect transistors for their excellent noise characteristics, and is shown in Figure 4. The FET pre-amp is followed by the post-amplifier shown in Figure 5.

The complete amplifier has a frequency band-pass with a center frequency of 160 kilocycles and a width of about 220 kilocycles. The midband gain is 15,000 and the equivalent noise input is about two microvolts. These characteristics are adequate for the ion chamber proposed. While the total power consumption is 100 milliwatts with the present design, it is estimated that a 30-milliwatt consumption can readily be obtained.

The circuit has been operated with the preliminary chamber design, but all that could be established was that it did not contribute to the rather poor resolution observed.

IV. Future Plans

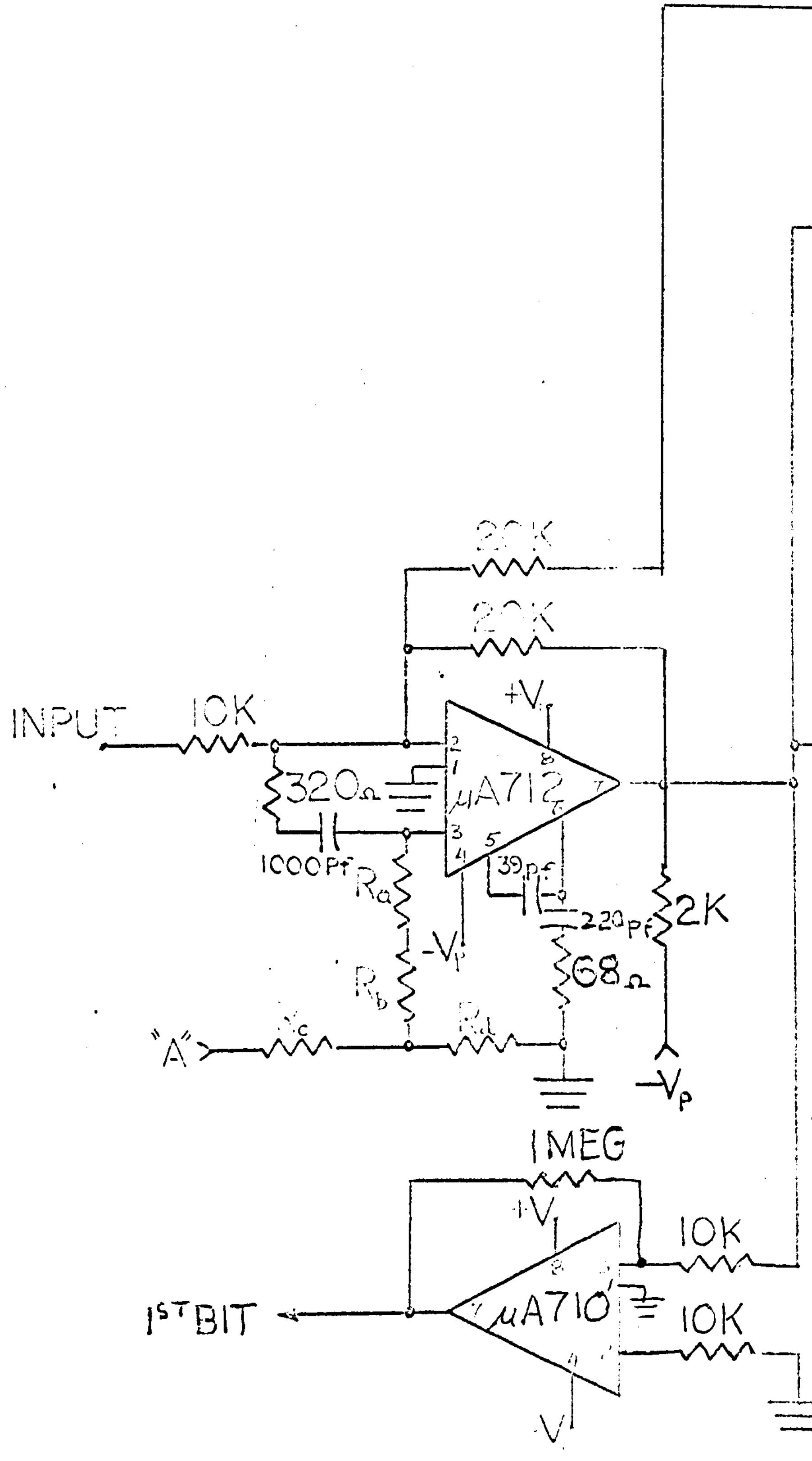
A. Completion of breadboard OSO-G model.

B. Construction of data handling circuitry for OSO-G breadboard model.

C. Construction and test of revised ion chamber.

D. Preparation of balloon flight hardware for balloon test of OSO-G breadboard model.

1ST STAGE

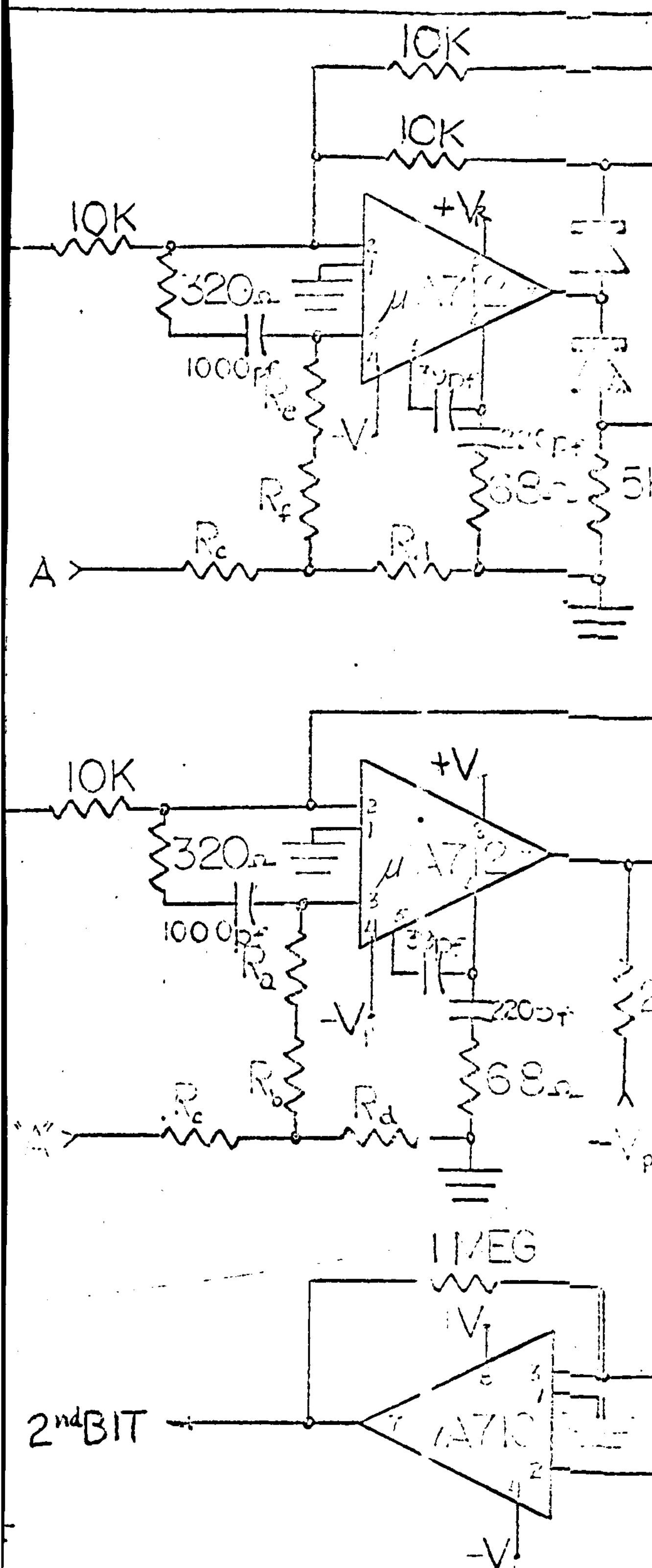


BIAS RESISTORS
$R_a \approx 5K$
$R_b \approx 1.6K$

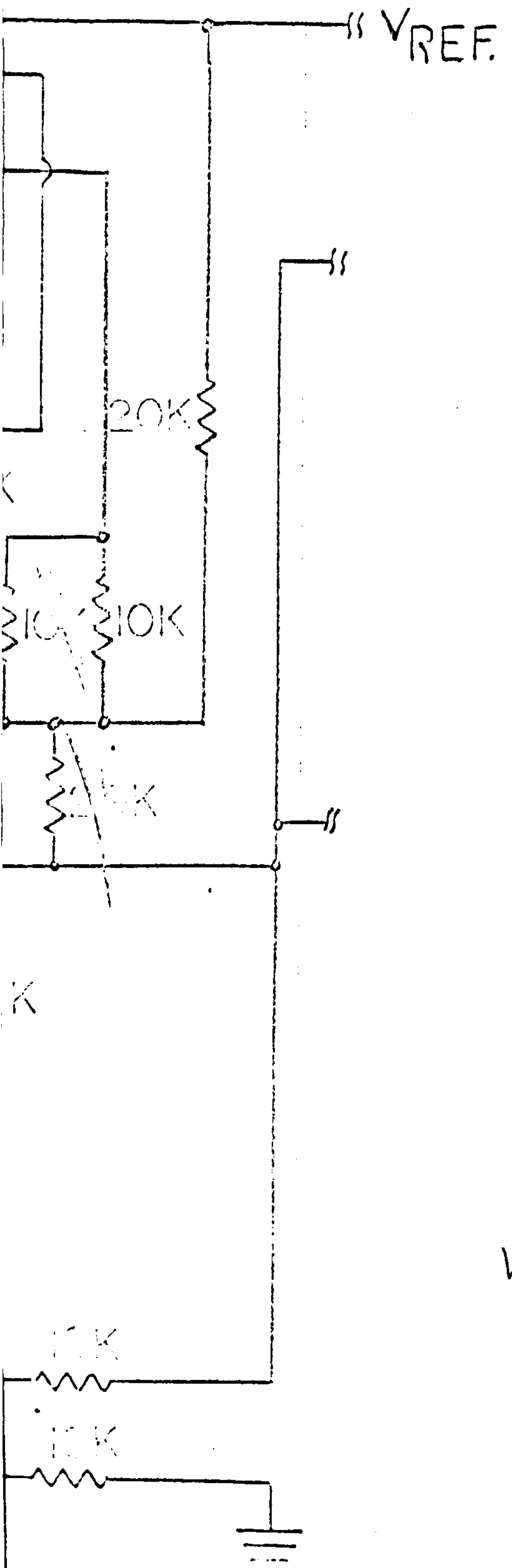
FIG

#1

2nd STAGE


10K
10K
10K
+V1
320Ω
1000pf
μA712
30pf
220pf
68Ω
Re
Rf
-V1
Rc
A
10K
+V1
320Ω
1000pf
Ra
μA712
30pf
220pf
Rb
68Ω
Rc
Rd
"A"
-V1
1 MEG
V1
2nd BIT
A710
-V1

1

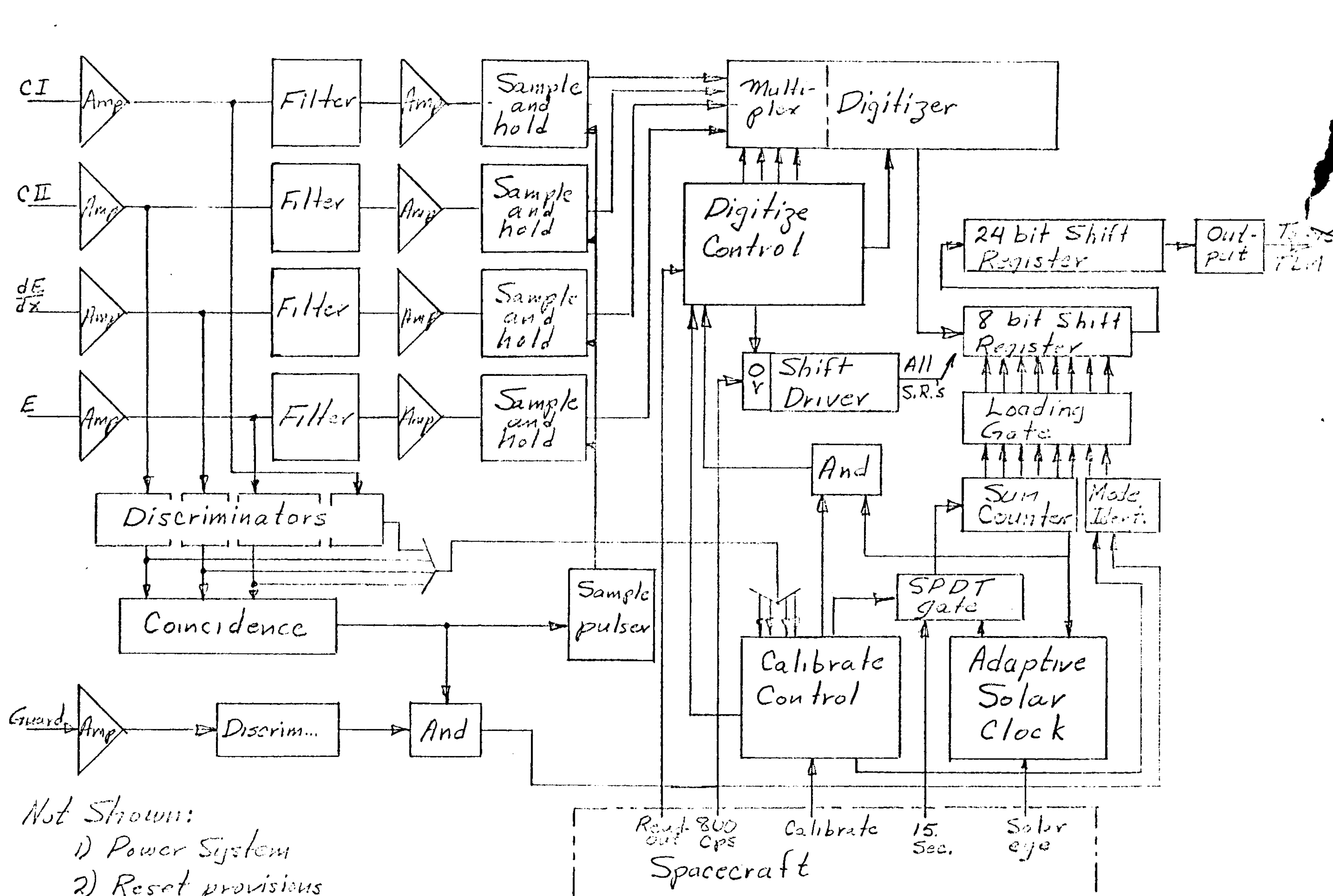


6 STAGES IDENTICAL
TO 2nd STAGE

$$V_{OUT} = -2|V_{n}| + V_{REF}$$

FOR 100 µS
.318 MW

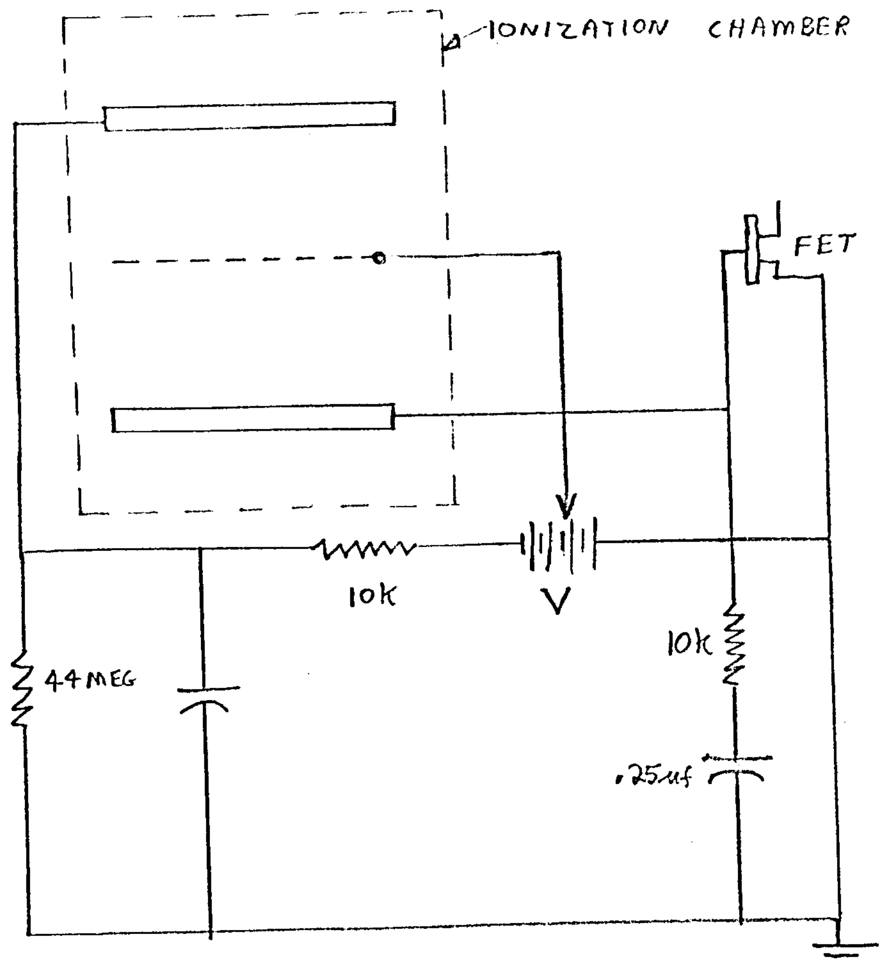
#3



Not Shown:

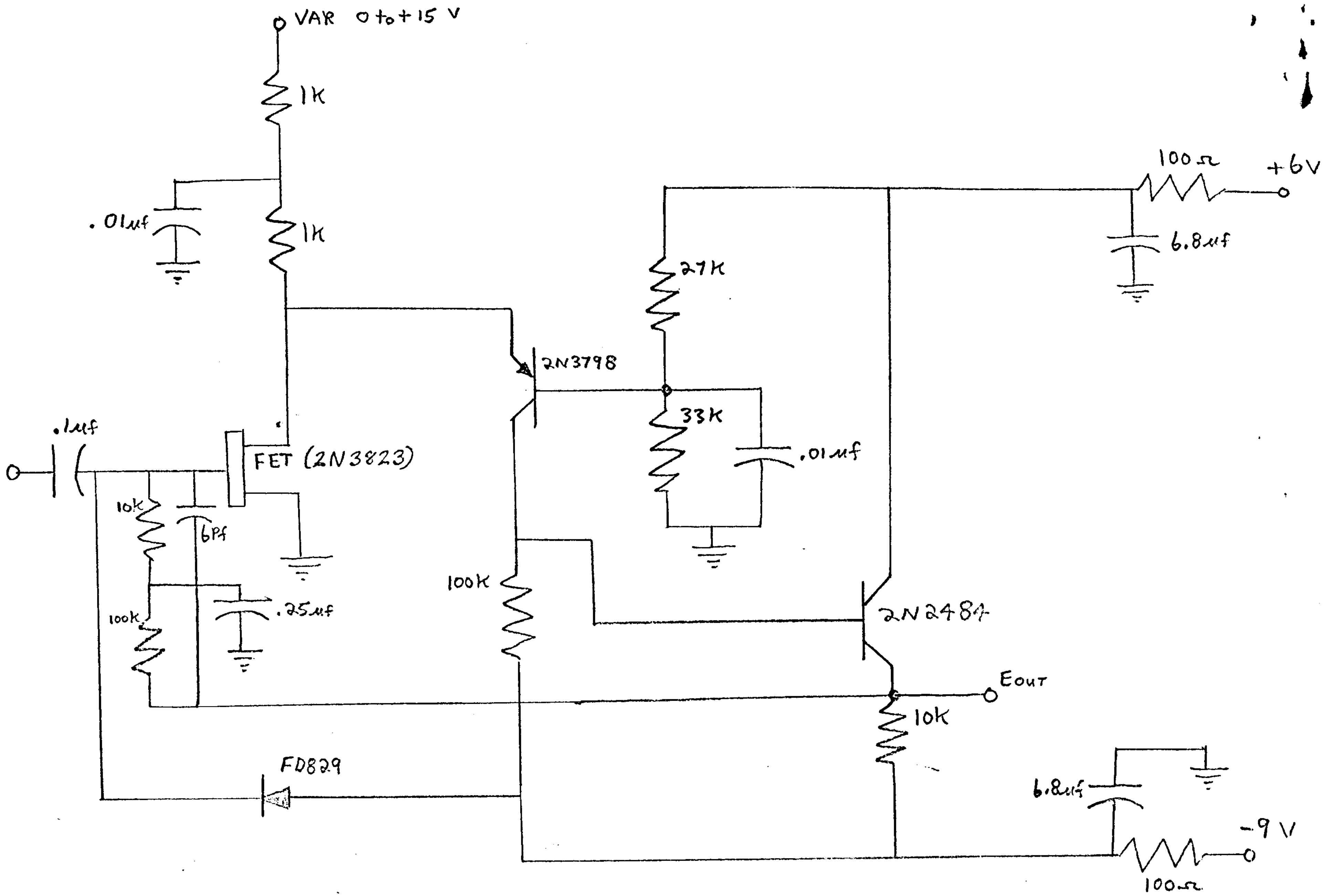
1) Power System
2) Reset provisions
3) Parity System (using 12 words of DSM)

FIG 2



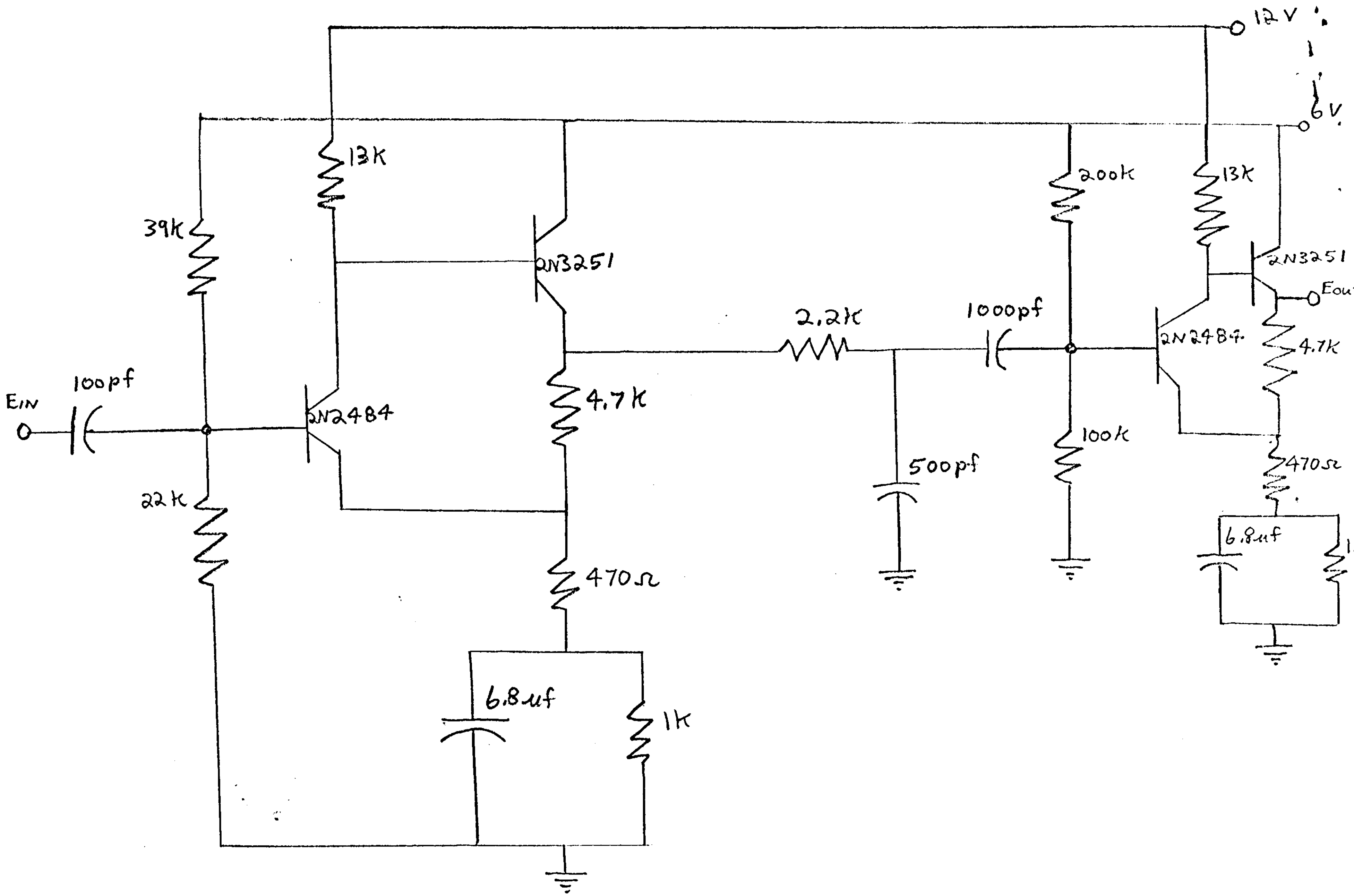
HOOKUP OF IONIZATION CHAMBER
TO LOW NOISE PREAMP

FIG 3



LOW NOISE PRE-AMP

FIG. 4



2^{ND} STAGE AMPLIFIER

FIG. 5